EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	488	ARIMILLI-RAVI-KUMAR.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 18:47
S2	0	ARIMILLI-RAVI.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:34
S3	197	GUTHRIE-GUY-LYNN.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:34
S4	2	GUTHRIE-GUY.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:34
S5	7	SHEN-HUGH.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:35
S6	161	WILLIAMS-DEREK-EDWARD.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:35
S7	22	WILLIAMS-DEREK.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:35
S8	4	(S1 S2 S3 S4 S5 S6) and STQ.clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:39

EAST Search History

S9	3	(S1 S2 S3 S4 S5 S6) and RC.clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:40
S10	15	(S1 S2 S3 S4 S5 S6) and (store adj queue).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:43
S11	13	((store near2 queue) STQ) same tenure	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:53
S13	25	((store near2 queue) STQ) and (updat$3 with ((full entire) near2 cache near2 line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:50
S14	996	((store near2 queue) STQ) and address near3 operation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:51
S15	3	((store near2 queue) STQ) and "address-only operation"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 15:52
S16	56	"address-only operation"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:41
S17	5	((store near2 queue) STQ) same data near2 tenure	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 10:32

EAST Search History

S18	301	((store near2 queue) STQ) same dispatch$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 10:40
S19	4528	711/117,118,122,133,141.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 10:35
S20	8	S18 and S19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 10:37
S21	5205	(711/117,118,122,133,141 710/54, 310).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 10:37
S22	12	S18 and S21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 10:37
S24	25	((store near2 queue) STQ) same granule	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:16
S25	1870	((store near2 queue) STQ) and "AND"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:16
S26	521	((store near2 queue) STQ) and ("AND" near3 (logic gate))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:31

EAST Search History

S27	5205	(711/117,118,122,133,141 710/54, 310).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:17
S28	31	S26 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:17
S29	517	((store near2 queue) STQ) and ("AND" near2 (logic gate))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:31
S30	19	((store near2 queue) STQ) and ("AND near2 gate" "AND near2 logic" "logically ANDing")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:32
S31	61	((store near2 (queue buffer)) STQ) and ("AND near2 gate" "AND near2 logic" "logically ANDing")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:38
S32	1	S31 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:37
S33	19	((store near2 (queue buffer)) STQ) same (full near2 entry)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:42
S34	247	((store near2 (queue buffer)) STQ) same (updat$3 with (cache near2 line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 14:08

EAST Search History

S35	17	S34 and (address near2 only)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 13:48
S36	13	((store near2 (queue buffer)) STQ) same (updat$3 with ((entire full all) near2 cache near2 line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 14:10
S37	5	((store near2 (queue buffer)) STQ) same (updat$3 with ((entire) near2 cache near2 line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:53
S38	46	(updat$3 with ((entire) near2 cache near2 line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:53
S39	82	(updat$3 with (entire with cache with line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:57
S40	62966	(((store write) near2 (queue buffer)) STQ)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:56
S41	62	S39 and S40	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:55
S42	6	S39 same S40	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:56

EAST Search History

S43	46988	((store near2 (queue buffer)) STQ)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:58
S44	5	S39 same S43	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:57
S45	371	(writ$4 with (entire with cache with line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:59
S46	9	S45 same S43	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:57
S47	44401	store near2 (queue buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 16:18
S48	754	(updat$4 writ$4) with (entire full whole) with cache with line	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:59
S49	29	S47 same S48	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 15:59
S50	133	("4136386" | "4167779" | "4167782" | "4225922" | "4323968" | "4349871" | "4354232" | "4425615" | "4442487" | "4445174" | "4467414" | "4484267" | "4755930" | "4823259").PN. OR ("5023776").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/06/02 16:07

EAST Search History

S51	273	S47 and "entire cache line"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 16:19
S52	42	S47 same "entire cache line"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:08
S53	89	(determin$4 with dispatch$4) same S47	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:15
S54	4	(determin$4 with dispatch$4) same S47 same RC	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:10
S55	2	(determin$4 with dispatch$4) same S47 same S48	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:11
S56	6	(determin$4 with dispatch$4) same S47 and S48	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:11
S57	5	(determin$4 with dispatch$4 with line) same S47	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:12
S58	56	S53 and ("711" "710" "712").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:12

EAST Search History

S59	1	S53 and ("AND near2 gate" "AND near2 logic" "logically ANDing")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:13
S61	56	S58 and (logic)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:14
S62	19	(determin$4 with dispatch$4) same S47 same logic$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/02 17:15
S63	56	"address-only operation"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 12:25
S64	2	S63 with permission	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 12:25
S65	2205	write near2 permission	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 12:26
S66	182	S65 with address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 12:33
S67	4528	711/117,118,122,133,141.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 12:26

EAST Search History

S68	9	S66 and S67	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 12:26
S69	4	S66 same (updat$4 with line)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 16:29
S72	5	S66 same (updat$4 with cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 12:35
S73	2205	write near2 permission	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 16:29
S74	182	S73 with address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 16:29
S75	5	S74 same invalidat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/05 16:30
S76	5	("20020112130" | "5924119" | "6484242").PN. OR ("6678799"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/06/05 17:50
S77	44456	store near2 (queue buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 15:47
S78	413	S77 same ("AND" near2 (gate logic))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 15:48

EAST Search History

S79	323	S77 same ("AND" near2 (gate logic))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/06/06 15:48
S80	310	S77 same ("AND" adj (gate logic))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/06/06 15:58
S81	5213	(711/117,118,122,133,141 710/54, 310).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 15:48
S82	10	S80 and S81	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/06/06 15:48
S83	17	S77 same ("AND" adj (gate logic)) same full	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/06/06 15:58
S84	26	(write adj permission) same invalidat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 18:50
S85	754	(updat$4 writ$4) with (entire full whole) with cache with line	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 18:48
S86	3	S84 and S85	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 18:48

EAST Search History

S87	308	(permission) same invalidat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:02
S88	3	S87 same S85	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 18:50
S89	12	(permission) same invalidat$4 same miss	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 20:09
S91	15	(permission) same S85	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:12
S92	56	"address-only operation"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:41
S93	2	S92 same permission	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:41
S94	3	S92 same invalidat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:42
S95	1	S92 same miss	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:43

EAST Search History

S96	10	S85 same stale	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:54
S97	139	S85 same invalidat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:54
S98	149	S85 same miss	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:54
S99	26	S85 same invalidat$4 same miss	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 19:58
S102	113	owner$4 same invalidat$4 same miss	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 20:09
S103	2	owner$4 same invalidat$4 same miss same stale	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 20:09

Tue, 6 Jun 2006, 10:33:09 PM EST

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- Combine search queries using AND, OR, or NOT
- Delete a search
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Search Query Display

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#1	((store queue)<in>metadata)	18
#2	(((store queue) <paragraph> (~~and~~ gate))<in>metadata)	0
#3	(((store queue) <paragraph> (~~and~~ logic))<in>metadata)	3
#4	(((store queue) <paragraph> (~~and~~ logic))<in>metadata)	3
#5	((cache update)<in>metadata)	12
#6	((updating cache)<in>metadata)	10

Results for "(((store queue) <paragraph> ('and' logic))<in>metadata)" e-mail printer friendly
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(((store queue) <paragraph> ('and' logic))<in>metadata) Search

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Energy efficient comparators for superscalar datapaths**
Ponomarev, D.V.; Kucuk, G.; Ergin, O.; Ghose, K.;
Computers, IEEE Transactions on
Volume 53, Issue 7, July 2004 Page(s):892 - 904
Digital Object Identifier 10.1109/TC.2004.29
AbstractPlus | References | Full Text: PDF(1112 KB) **IEEE JNL**
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2. **Software-hardware cooperative memory disambiguation**
Huang, R.; Garg, A.; Huang, M.;
High-Performance Computer Architecture, 2006. The Twelfth International Symposium on
11-15 Feb. 2006 Page(s):244 - 253
Digital Object Identifier 10.1109/HPCA.2006.1598133
AbstractPlus | Full Text: PDF(472 KB) **IEEE CNF**
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3. **Power efficient comparators for long arguments in superscalar processors**
Ponomarev, D.; Kucuk, G.; Ergin, O.; Ghose, K.;
Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on
25-27 Aug. 2003 Page(s):378 - 383
Digital Object Identifier 10.1109/LPE.2003.1231928

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Result # 1 Relevance: ○○○○○

Modified Cache Update Cycle for Intel 82385 Based Systems

1990-08-01 IPCOM000101599D English (United States)

This article describes a technique for interfacing a 64-bit-wide memory bus to a 32-bit-wide cache bus on Intel 82385 cache controller based systems.

Result # 2 Relevance: ○○○○○

Optimized Cache Update

2004-07-08 IPCOM000029683D English (United States)

Optimized Cache Update

Result # 3 Relevance: ○○

32-Bit (ECC) Partial Write Data Conversion with a Cache Memory System

1992-10-01 IPCOM000110038D English (United States)

This article describes a method for use in a computer system to solve the partial write performance penalty by converting partial memory write cycles to full memory write cycles if the addresed memory location is in the cache memory subsystem. This assumes that ECC is ...

Result # 4 Relevance: ○○

Avoiding XI in Mp Systems Using Software Locks

1989-12-01 IPCOM000037333D English (United States)

In multiprocessing systems the degradation due to cross interrogation on shared data can be avoided for a class of locked data. The nature of the management of the cache coherency in this case is detailed. In addition, the possible use of a particular strategy based on ...

Result # 5 Relevance: ○

System Reset Protection Synchronous Cache System Destaging

1983-04-01 IPCOM000045687D English (United States)

This invention relates to a method for inhibiting the SYSTEM RESET INTERRUPTION by a CPU of DASD (direct-access storage device) to cache destaging within a storage subsystem initiated by another CPU in a multi-CPU shared access storage subsystem environment. The method ...

Result # 6 Relevance:

A Navigation Method and System for On-demand Paging of Search Results in Applications on Application Servers

2003-11-04 IPCOM000020235D English (United States)

Disclosed is a navigation method and system for on-demand paging of search results in applications on application servers to manage a very large result set from a query issued to the database, maximize performance and taking data consistency, scalability and session ...

Result # 7 Relevance:

Switching Pattern Control in an Electron Beam Writing System Between Bidirectional and Unidirectional Writing Without Altering Pattern Drive Code

1977-09-01 IPCOM000089071D English (United States)

The basic electron-beam writing system exposes patterns on a target or wafer on alternating forward and backward scans of the writing field, as shown in Fig. 1A. This allows relatively slow, narrow-bandwidth magnetic deflection signals, but requires precise adjustment of ...

Result # 8 Relevance:

A Cache Technique for Synchronization Variables in Highly Parallel, Shared Memory Systems

1988-12-31 IPCOM000128199D English (United States)

Caches have traditionally been used to lower the average latency of memory access. When paired with the individual CPUs of a multiprocessor, they have the additional benefit of reducing the overall load on the processor-memory interconnection. Since synchronization ...

Result # 9 Relevance:

Batched Store Broadcast in MP Caches

1991-11-01 IPCOM000122191D English (United States)

Disclosed is a technique for implementing data broadcasting in multiprocessor systems with shared memory. The key approach proposed is to employ data buffering so that broadcasting traffic may be reduced.

Result # 10 Relevance:

Long Thin Networks (RFC2757)

2000-01-01 IPCOM000003354D English (United States)

In view of the unpredictable and problematic nature of long thin networks (for example, wireless WANs), arriving at an optimized transport is a daunting task. We have reviewed the existing proposals along with future research items. Based on this overview, we also recommend ...

Displaying page 1 of 1 << FIRST | < BACK | NEXT > | LAST >>

Search query: cache update

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June 06, 2006 USPTO

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Displaying records #1 through 4 out of 4

Result # 1 Relevance: ○○○○○

MRU Update Control for Multiple Level Caches

1991-11-01 IPCOM000122134D English (United States)

Disclosed is a technique for updating cache line activeness between different cache hierarchies. The central idea is to periodically update certain MRU information of first level cache to second level. The control of update may utilize free first level cache directory ...

Result # 2 Relevance: ○○○○○

Updating Cache Data Array's with Data Stored by Other CPU's

1976-07-01 IPCOM000086100D English (United States)

This description explains how data and addresses can be broadcasted to other CPU's from a CPU doing a backing storage store operation.

Result # 3 Relevance: ○○

Method for improving cache utilization during potentially slow update operations

2005-05-19 IPCOM000125126D English (United States)

The utilization of a cache can be negatively impacted when the updates to cache entries take an indeterminate amount of time. The cache utilization can be improved by setting a state value in the cache entry to indicate that an update is pending and releasing resources used ...

Result # 4 Relevance: ○

T/TCP -- TCP Extensions for Transactions Functional Specification (RFC1644)

1994-07-01 IPCOM000002480D English (United States)

This memo specifies T/TCP, an experimental TCP extension for efficient transaction-oriented (request/response) service. This backwards-compatible extension could fill the gap between the current connection-oriented TCP and the datagram-based UDP.

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